Triple Differential Receiver with 300m Adjustable Line Equalization

Preliminary Technical Data

AD8122

FEATURES

- Compensates cables to 300 meters for wideband video
  - 60 MHz Equalized BW @ 300 meters of UTP Cable
  - 120 MHz Equalized BW @ 150 meters of UTP Cable
- Fast time domain performance
  - 70 ns settling time to 1% with 300 meters of UTP cable
  - 7 ns rise/fall times with 2 V step @ 300 meters of UTP cable
- Three frequency response gain adjustment pins
  - High frequency peaking adjustment (V_{PEAK})
  - Output lowpass filter cutoff adjustment (V_{FILTER})
  - Broadband flat gain adjustment (V_{GAIN})
- Selectable for UTP or coax compensation
- DC output offset adjust (V_{OFFSET})
- Low output offset voltage: ±4 mV @ G = 1
- Compensates both RGB and YPbPr
- Two on-chip comparators with hysteresis
  - Can be used for common-mode sync extraction
- Available in 40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

- Keyboard-video-mouse (KVM)
- Digital signage
- RGB video over UTP cables
- Professional video projection and distribution
- HD video
- Security video

FUNCTIONAL BLOCK DIAGRAM

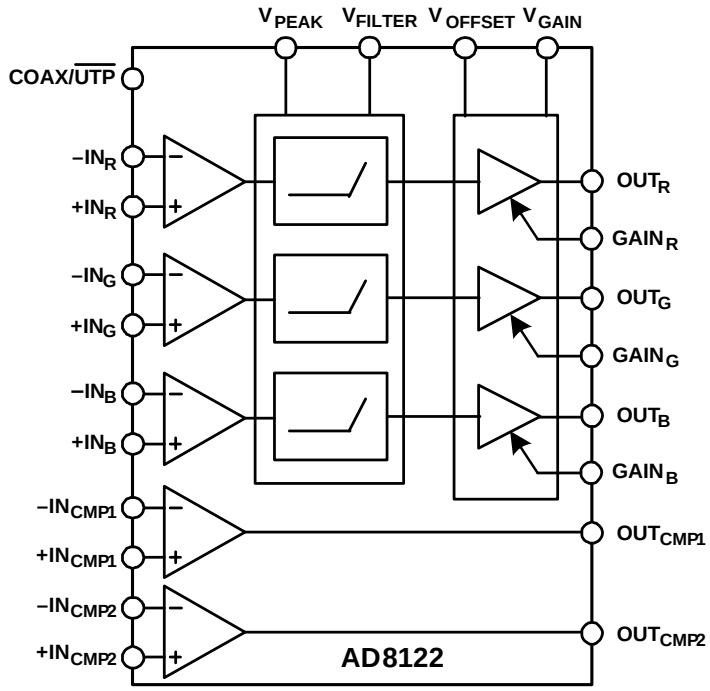

Figure 1.

GENERAL DESCRIPTION

The AD8122 is a triple, high speed, differential receiver and equalizer that compensates for the transmission losses of UTP and coaxial cables up to 300 meters in length. Various gain stages are summed together to best approximate the inverse frequency response of the cable. Each channel features a high impedance differential input that is ideal for interfacing directly with the cable.

The AD8122 has two control inputs for optimal cable compensation, one LPF control input, an input to select between UTP and coax cable, and an output offset adjust input. The cable compensation inputs are used to compensate for different cable lengths; the V_{PEAK} input controls the amount of high frequency peaking and the V_{GAIN} input adjusts the broadband flat gain, which compensates for the flat cable loss. The V_{FILTER} input controls the cutoff frequency of output lowpass filters on each channel. Selection between UTP and coaxial cable compensation responses is determined by the binary COAX/$\overline{\text{UTP}}$ input, which can be left floating in UTP applications. The V_{OFFSET} pin allows the dc voltage at the output to be adjusted, which can be useful in dc-coupled systems.

For added flexibility, the gains of each channel can be set to x1 or x2 using the associated GAIN control pins.

The AD8122 is available in a 6 mm × 6 mm, 40-lead LFCSP and is rated to operate over the extended temperature range of −40°C to +85°C.

Rev. PrC

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SPECIFICATIONS

T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, G = 2, Belden Cable (BL-7987R), V_{OFFSET} = 0 V, V_{PEAK} and V_{GAIN} are set to optimum settings, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC AND NOISE PERFORMANCE					
−3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p, AD8122 alone		155		MHz
	V_{OUT} = 2 V p-p, 150 meters Cat-5		110		MHz
	V_{OUT} = 2 V p-p, 300 meters Cat-5		57		MHz
	V_{OUT} = 1 V p-p, AD8122 alone, R_L = 1 KΩ, G = 1		260		MHz
	V_{OUT} = 1 V p-p, 150 meters Cat-5, R_L = 1 KΩ, G = 1		120		MHz
	V_{OUT} = 1 V p-p, 300 meters Cat-5, R_L = 1 KΩ, G = 1		60		MHz
Slew Rate	V_{OUT} = 2 V p-p, AD8122 alone				V/µsec
10% to 90% Rise/Fall Time	V_{OUT} = 2 V step, 150 meters Cat-5		6		ns
	V_{OUT} = 2 V step, 300 meters Cat-5		7		ns
	V_{OUT} = 1 V step, 150 meters Cat-5, R_L = 1 KΩ, G = 1		6		ns
	V_{OUT} = 1 V step, 300 meters Cat-5, R_L = 1 KΩ, G = 1		7		ns
Settling Time to 1%	V_{OUT} = 2 V step, 150 meters Cat-5				ns
	V_{OUT} = 2 V step, 300 meters Cat-5		70		ns
	V_{OUT} = 1 V step, 150 meters Cat-5, R_L = 1 KΩ, G = 1				ns
	V_{OUT} = 1 V step, 300 meters Cat-5, R_L = 1 KΩ, G = 1		70		ns
Integrated Output Voltage Noise	150 meter setting, integrated to 160 MHz		2.5		mV rms
	300 meter setting, integrated to 160 MHz		16		mV rms
INPUT PERFORMANCE					
Input Voltage Range	Single-ended, −IN and +IN		±4.0		V
Maximum Differential Voltage Swing			3		V p-p
Voltage Gain Error	G = 1, $\Delta V_O/\Delta V_I$, V_{GAIN} set for 0 meters of cable		2		%
	G = 2, $\Delta V_O/\Delta V_I$, V_{GAIN} set for 0 meters of cable		2		%
Channel-to-Channel Gain Matching	G = 1, V_{PEAK}, V_{GAIN} set for 300 meters of cable		0.2		%
	G = 2, V_{PEAK}, V_{GAIN} set for 300 meters of cable		0.2		%
Common-Mode Rejection (CMR)	At dc, V_{PEAK} = V_{GAIN} = 0 V, G = 1/G = 2		−92/−85		dB
	At dc, V_{PEAK}, V_{GAIN} set for 300 meters of cable				dB
	At 1 MHz, V_{PEAK}, V_{GAIN} set for 300 meters of cable				
	G = 1/G = 2		−66/−60		dB
	At 50 MHz, V_{PEAK}, V_{GAIN} set for 300 meters of cable				
	G = 1/G = 2		+4/+10		dB
	At 100 MHz, V_{PEAK}, V_{GAIN} set for 300 meters of cable				
	G = 1/G = 2		+8/+11		dB
Input Resistance	Common mode		4.4		MΩ
	Differential		3.7		MΩ
Input Capacitance	Common mode		1.0		pF
	Differential		0.5		pF
Input Bias Current			1.1		µA
V_{OFFSET} Pin Current			2.0		µA
V_{GAIN} Pin Current			1.0		µA
V_{PEAK} Pin Current			1.0		µA
V_{FILTER} Pin Current			1.0		µA
COAX/$\overline{UTP}$ Pin Current	Logic 0/Logic1		−1/24		µA
ADJUSTMENT PINS					
V_{PEAK} Input Voltage Range	Relative to GND		0 to 2		V
V_{GAIN} Input Voltage Range	Relative to GND		0 to 2		V
V_{OFFSET} to OUT Gain	Range limited by output swing, G = 1, V_{GAIN} = 0V		1		V/V

Parameter	Conditions	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Voltage Swing			−3.9 to +3.9		V
	R_L = 1 KΩ, G = 1				V
Output Offset Voltage	RTO, $V_{PEAK} = V_{GAIN} = V_{FILTER} = V_{OFFSET}$ = 0 V, G = 1,				
	R_L = 1 KΩ		±4		mV
	RTO, Control inputs set for 300 meters of cable				mV
Output Offset Voltage Drift	RTO				µV/°C
POWER SUPPLY					
Operating Voltage Range		±4.5		±5.5	V
Positive Quiescent Supply Current			120		mA
Negative Quiescent Supply Current			66		mA
Supply Current Drift, I_{CC}/I_{EE}					µA/°C
Positive Power Supply Rejection Ratio	DC, referred to output		−70		dB
	100 MHz, referred to output				dB
Negative Power Supply Rejection Ratio	DC, referred to output		−81		dB
	100 MHz, referred to output				dB
Power Down, V_{IH} (Minimum)	Minimum Logic 1 voltage		1.1		V
Power Down, V_{IL} (Maximum)	Maximum Logic 0 voltage		0.8		V
Positive Supply Current, Powered Down	$V_{PEAK} = V_{GAIN} = V_{POLE}$ = 0 V		3.4		mA
Negative Supply Current, Powered Down	$V_{PEAK} = V_{GAIN} = V_{POLE}$ = 0 V		0.4		mA
COMPARATORS					
Output Voltage Levels	V_{OH}/V_{OL}		3.33/0.33		V
Hysteresis	V_{HYST}		73		mV
Propagation Delay	$t_{PD, LH}/t_{PD, HL}$		14/10		ns
Rise/Fall Times	t_{RISE}/t_{FALL}		10/7		ns
Output Resistance					Ω
OPERATING TEMPERATURE RANGE		−40		+85	°C

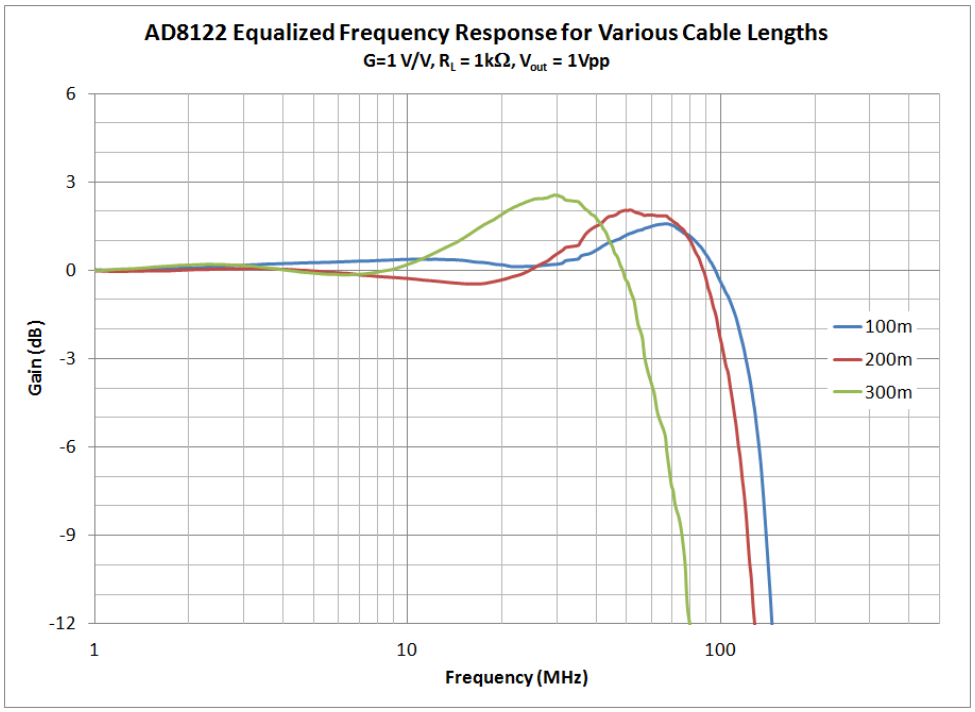


Figure 2. Equalized Frequency Response for Various Cable Lengths

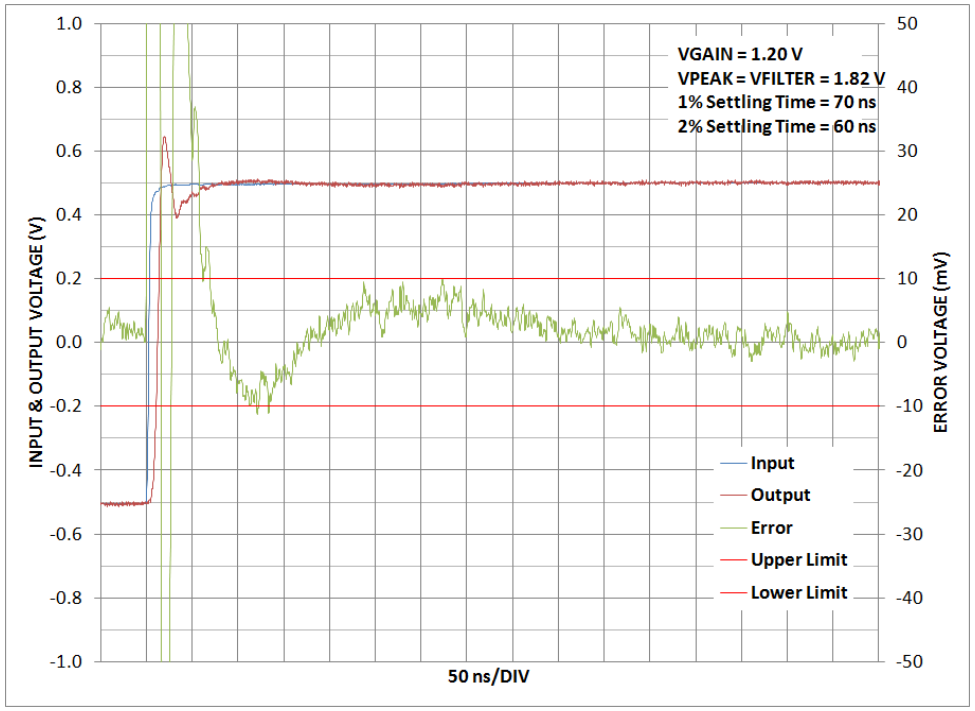


Figure 3. Settling Time, G = 1, R_L = 1KΩ

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 4
Input Voltage (Any Input)	V_{S-} – 0.3 V to V_{S+} + 0.3 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board in still air.

Table 3. Thermal Resistance with the Underside Pad Connected to the Plane

Package Type/PCB Type	θ_{JA}	Unit
40-Lead LFCSP/4-Layer	TBD	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the AD8122 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8122. Exceeding a junction temperature of 175°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipation due to each load current is calculated by multiplying the load current by the voltage difference between the associated power supply and the output voltage. The total power dissipation due to load currents is then obtained by taking the sum of the individual power dissipations. RMS output voltages must be used when dealing with ac signals.

Airflow reduces θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a solid plane (usually the ground plane) to achieve the specified θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 40-lead LFCSP (29°C/W) on a JEDEC standard 4-layer board with the underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

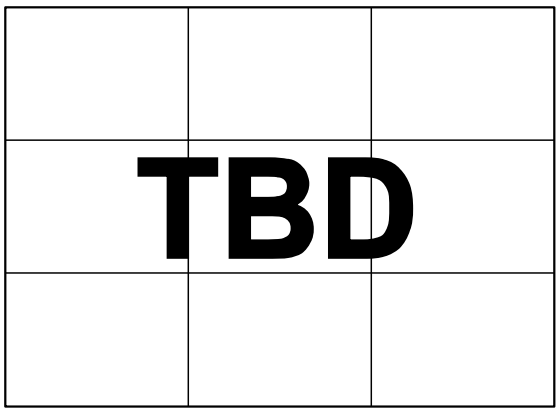


Figure 4. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

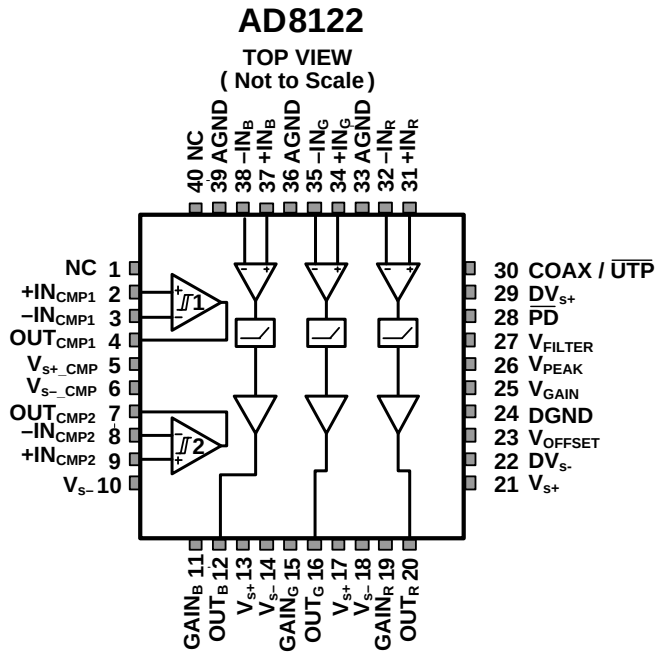


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 40	NC	No Internal Connection.
2	$+IN_{CMP1}$	Positive Input, Comparator 1.
3	$-IN_{CMP1}$	Negative Input, Comparator 1.
4	OUT_{CMP1}	Output, Comparator 1.
5	V_{S+_CMP}	Positive Power Supply, Comparator. Connect to +5V.
6	V_{S-_CMP}	Negative Power Supply, Comparator. Connect to −5V.
7	OUT_{CMP2}	Output, Comparator 2.
8	$-IN_{CMP2}$	Negative Input, Comparator 2.
9	$+IN_{CMP2}$	Positive Input, Comparator 2.
10, 14, 18	V_{S-}	Negative Power Supply, Equalizer Sections. Connect to −5V.
11	$GAIN_B$	Blue Channel Gain. Connect to OUT_B for G = 1; connect to GND for G = 2.
12	OUT_B	Output, Blue Channel.
13, 17, 21	V_{S+}	Positive Power Supply, Equalizer Sections. Connect to +5V.
15	$GAIN_G$	Green Channel Gain. Connect to OUT_G for G = 1; connect to GND for G = 2.
16	OUT_G	Output, Green Channel.
19	$GAIN_R$	Red Channel Gain. Connect to OUT_R for G = 1; connect to GND for G = 2.
20	OUT_R	Output, Red Channel.
22	DV_{S-}	Negative Power Supply, Digital Control. Connect to −5V.
23	V_{OFFSET}	Output Offset Control Voltage.
24	DGND	Digital Ground Reference.
25	V_{GAIN}	Broadband Flat Gain Control Voltage.
26	V_{PEAK}	Equalizer High Frequency Boost Control Voltage.
27	V_{FILTER}	Lowpass Filter Cutoff Frequency Adjustment Control Voltage.

28	$\overline{PD}$	Power Down.
29	DV_{S+}	Positive Power Supply, Digital Control. Connect to +5V.
30	COAX/$\overline{UTP}$	Cable Compensation Control Input. Connect to Logic 1 for Coax, Logic 0 for UTP.
31	$+IN_R$	Positive Input, Red Channel.
32	$-IN_R$	Negative Input, Red Channel.
33, 36, 39	AGND	Analog Ground Reference
34	$+IN_G$	Positive Input, Green Channel.
35	$-IN_G$	Negative Input, Green Channel.
37	$+IN_B$	Positive Input, Blue Channel.
38	$-IN_B$	Negative Input, Blue Channel.
Exposed Underside Pad		Thermal Plane Connection. Connect to any PCB plane with voltage between V_{S+} and V_{S-}.

THEORY OF OPERATION

The AD8122 is a triple, wideband, low noise analog line equalizer that compensates for losses in UTP and coaxial cables up to 300 meters in length. The 3-channel architecture is targeted at high resolution RGB applications but can be used in HD YPbPr applications as well. The transfer function of theAD8122 can be pin-selected for UTP or coaxial cable, and the gain of each channel can be set to 1 or 2.

Four continuously adjustable control voltages, common to the RGB channels, are available to the designer to provide compensation for various cable lengths as well as for variations in the cable itself. The V_{PEAK} input is used to control the amount of high frequency peaking. V_{PEAK} is the control that is used to compensate for frequency and cable-length dependent, high frequency losses that are present due to the skin effect of the cable. A second control pin, V_{GAIN}, is used to adjust broadband gain to compensate for low frequency flat losses present in the cable. A third control pin, V_{FILTER}, is used to adjust the cutoff frequency of the output lowpass filters. Finally, an output offset adjust control, V_{OFFSET}, allows the designer to shift the output dc level.

The AD8122 has a high impedance differential input that makes termination simple and allows dc-coupled signals to be received directly from the cable. The AD8122 input can also be used in a single-ended fashion in coaxial cable applications. For differential systems that require very wide input common-mode range, the AD8143 high-voltage triple differential receiver can be placed in front of the AD8122.

The AD8122 has a low impedance output that is capable of driving a 150 Ω load. For systems where the AD8122 has to drive a high impedance capacitive load, it is recommended that a small series resistor be placed between the output and load to buffer the capacitance. The resistor should not be so large as to reduce the overall bandwidth to an unacceptable level.

Two comparators are provided on-chip that can be used for sync pulse extraction in systems that use sync-on-common mode encoding. Each comparator has very low output impedance and can therefore be used in a source-only cable termination scheme by placing a series resistor equal to the cable characteristic impedance directly on the comparator output. Additional details are provided in the Applications Information section.

INPUT SINGLE-ENDED VOLTAGE RANGE CONSIDERATIONS

When using the AD8122 as a receiver, it is important to ensure that its single-ended input voltages stay within their specified ranges. The received single-ended level for each input is calculated by adding the common-mode level of the driver, the single-ended peak amplitude of the received signal, the amplitude of any sync pulses, and the other induced common-mode signals, such as ground shifts between the driver and the AD8122 and pickup from external sources, such as power lines and fluorescent lights. See the Applications Information section for more details.

APPLICATIONS INFORMATION

BASIC OPERATION

The AD8122 is easy to apply because it contains everything on-chip needed for cable loss compensation. Figure 8 shows a basic application circuit (power supplies not shown) with common-mode sync pulse extraction that is compatible with the common-mode sync pulse encoding technique used in the AD8134, AD8142, AD8147, and AD8148 triple differential drivers. If sync extraction is not required, the terminations can be single 100 Ω resistors, and the comparator inputs can be left floating.

INPUT OVERDRIVE RECOVERY AND PROTECTION

Occasional large differential transients can occur on the cable due to a number of causes, such as ESD and switching. When operating the AD8122 at G = 1, a differential input that exceeds +3.4V or -3.4V will cause the output to "stick" at the associated power supply rail (positive rail for positive overdrive, negative rail for negative overdrive). The AD8122 recovers from this condition when the magnitude of the differential input falls below 200 mV. Most video signals return to nominally zero volts during the blanking intervals, therefore recovery from the overdriven condition in systems that use these signals would occur during the first blanking interval that occurs after the overdrive event has passed. In systems with G = 1 that employ video signals that do not return to zero, such as those that include DC offsets, it is necessary to prevent the overdrive condition from occurring. In these cases the protection circuit illustrated in Figure 6, which limits the differential input voltage to a little over ±2V, should be placed between the termination resistors and each AD8122 differential input. The overdrive condition does not occur in applications with G = 2.

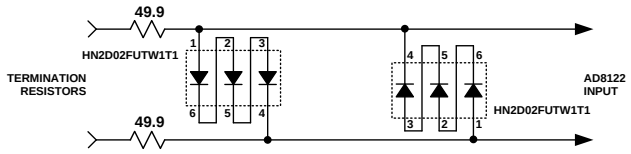


Figure 6. Required Input Protection For Applications With G = 1

COMPARATORS

While the two on-chip comparators are most often used to extract video sync pulses from the received common-mode voltages as shown in Figure 8, they may also be used to recover sync pulses in sync-on-color applications, to receive differential digital information received on other channels such as the fourth UTP pair , or as general purpose comparators. Built-in hysteresis helps to eliminate false triggers from noise. The Sync Pulse Extraction Using Comparators section describes the sync extraction details.

The comparator outputs have nearly 0 Ω output impedance and are designed to drive source-terminated transmission lines. The source termination technique uses a resistor in series with each comparator output such that the sum of the comparator source resistance (≈0 Ω) and the series resistor equals the transmission line characteristic impedance. The load end of the transmission line is high impedance. When the signal is launched into the source termination, its initial value is one-half of its source value because its amplitude is divided by two in the voltage divider formed by the source termination and the transmission line. At the load, the signal experiences nearly 100% positive reflection due to the high impedance load and is restored to nearly its full value. This technique is commonly used in PCB layouts that involve high speed digital logic.

Figure 7 shows how to apply the comparators with source termination when driving a 50 Ω transmission line that is high impedance at its receive end.

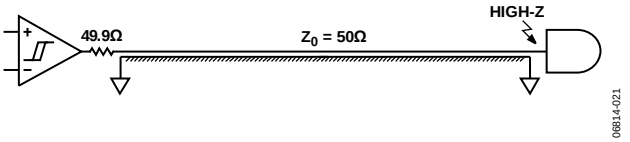


Figure 7. Using Comparator with Source Termination

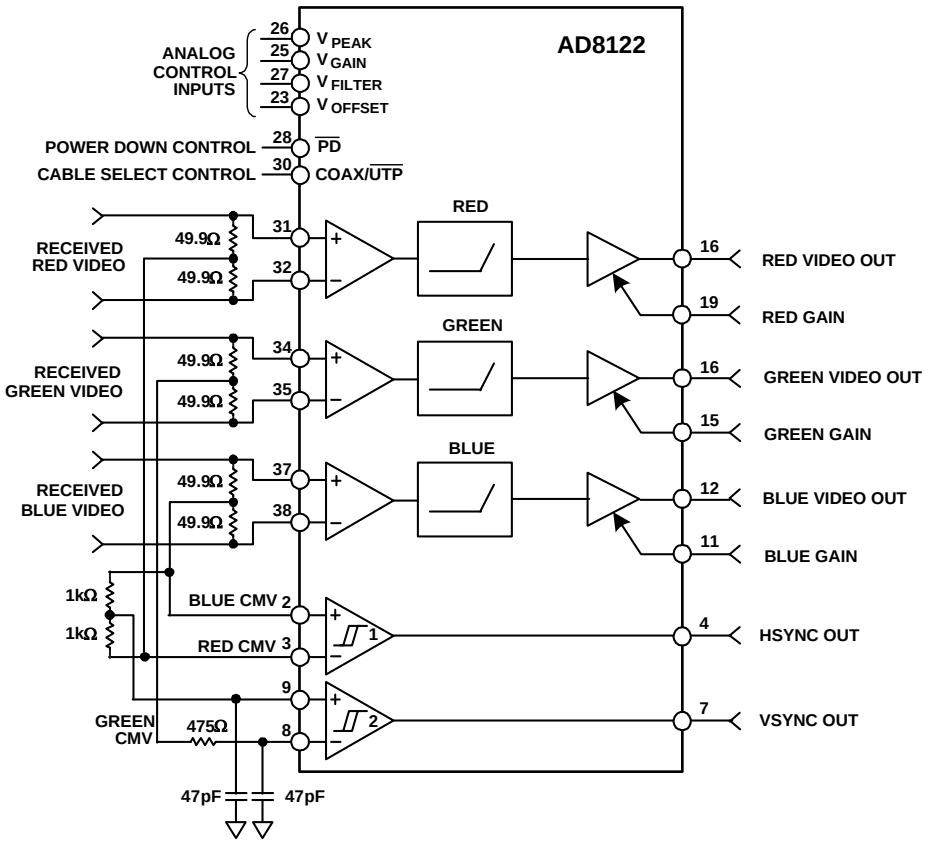


Figure 8. Basic Application Circuit with Common-Mode Sync Extraction (supplies and input protection not shown)

SYNC PULSE EXTRACTION USING COMPARATORS

The AD8122 is useful in many systems that transport computer video signals, which are typically comprised of red, green, and blue video signals and separate horizontal and vertical sync signals (RGBHV). Because the sync signals are separate and not embedded in the color signals, it is advantageous to transmit them using a simple scheme that encodes them among the three common-mode voltages of the RGB signals. The AD8134, AD8142, AD8147, and AD8148 triple differential drivers are natural complements to the AD8122 because they perform the sync pulse encoding with the necessary circuitry on-chip.

The sync encoding equations follow:

$$Red\ V_{CM} = \frac{K}{2}\left[V - H\right] \quad (1)$$

$$Green\ V_{CM} = \frac{K}{2}\left[-2\ \mathrm{V}\right] \quad (2)$$

$$Blue\ V_{CM} = \frac{K}{2}\left[V + H\right] \quad (3)$$

where:
Red V_{CM}, *Green* V_{CM}, and *Blue* V_{CM} are the transmitted common-mode voltages of the respective color signals.
K is an adjustable gain constant that is set by the driver.
V and H are the vertical and horizontal sync pulses, defined with a weight of −1 when the pulses are in their low states, and a weight of +1 when they are in their high states.

The AD8134, AD8142 and AD8146/AD8147/AD8148 data sheets contain further details regarding the encoding scheme. Figure 8 illustrates how the AD8122 comparators can be used to extract the horizontal and vertical sync pulses that are encoded on the RGB common-mode voltages by the aforementioned drivers.

USING THE V_{PEAK}, V_{GAIN}, V_{FILTER}, AND V_{OFFSET} INPUTS

The V_{PEAK} input is the main peaking control and is used to compensate for the low-pass roll-off in the cable response. The V_{GAIN} input controls the wideband flat gain and is used to compensate for the cable loss that is nominally flat.

The output of each channel contains an on-chip adjustable lowpass filter to reduce high frequency noise. In most applications, the filter cutoff frequency control, V_{FILTER}, is connected directly to the V_{PEAK} voltage in order to provide maximum bandwidth and minimum noise for a given V_{PEAK} setting. External lowpass filters are generally not required.

The V_{OFFSET} input is used to produce an offset at the AD8122 output. The output offset is equal to the voltage applied to the V_{OFFSET} input, limited by the output swing limits.

USING THE COAX/$\overline{\text{UTP}}$ SELECTOR

Connect this input to Logic 1 (or +5V) for coaxial cable and Logic 0 (or GND) for UTP cable. This input has an internal pulldown resistor, and can therefore be left floating in UTP applications.

DRIVING HIGH-Z AND CAPACITIVE LOADS

In many RGB-over-UTP applications, delay correction is required to remove the skew that exists among the three pairs used to carry the RGB signals. The AD8120 is ideally suited to perform this skew correction, and can be placed immediately following the AD8122 in the receiver signal chain. The AD8120 has a high input impedance, and a fixed gain of two. When using the AD8120 with the AD8122, the AD8122 should be configured for a gain of one by connecting each video output to its respective "GAIN" pin.

When driving a high impedance capacitive input, it is necessary to place a small series resistor between each of the three AD8122 video outputs and the load to buffer the input capacitance of the device being driven. Clearly, the resistor value must be small enough to preserve the required bandwidth.

DRIVING 75 Ω CABLE WITH THE AD8122

When the RGB outputs must drive a 75 Ω line rather than a high impedance load, an additional gain of two is required to make up for the double termination loss (75 Ω source and load terminations). Each output of the AD8122 is easily configured for a gain of two by grounding the respective "GAIN" pin.

LAYOUT AND POWER SUPPLY DECOUPLING CONSIDERATIONS

Standard high speed PCB layout practices should be adhered to when designing with the AD8122. A solid ground plane is required and controlled impedance traces should be used when interconnecting the high speed signals. Source termination resistors on all of the outputs must be placed as close as possible to the output pins.

The exposed paddle on the underside of the AD8122 must be connected to a pad that connects to at least one PCB plane. Several thermal vias should be used to make the connection between the pad and the plane(s).

High quality 0.1 µF power supply decoupling capacitors should be placed as close as possible to all of the supply pins. Small surface-mount ceramic capacitors should be used for these, and tantalum capacitors are recommended for bulk supply decoupling.

INPUT COMMON-MODE RANGE

Most applications that use the AD8122 as a receiver use a driver (such as one from the AD8146/AD8147/AD8148 family, the AD8133, or the AD8134) powered from ±5 V supplies. This places the common-mode voltage on the line nominally at 0 V relative to the ground potential at the driver and provides optimum immunity from any common-mode anomalies picked up along the cable (including ground shifts between the driver and receiver ends). In many of these applications, the AD8122 input voltage range of typically ±4 V is sufficient. If wider input range is required, the AD8143 triple receiver (input common-mode range equals ±10.5 V on ±12 V supplies) may be placed in front of the AD8122. Figure 9 illustrates how this is done for one channel.

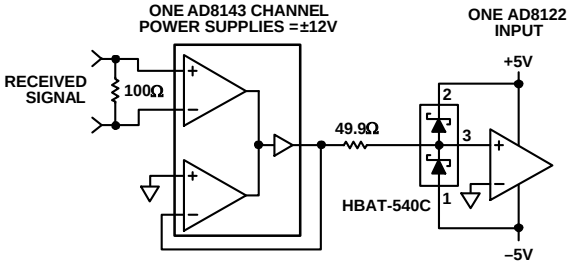


Figure 9. Optional Use of AD8143 in Front of AD8122 for Wide Input Common-Mode Range

The Schottky diodes are required to protect the AD8122 from any AD8143 outputs that may exceed the AD8122 input limits. The 49.9 Ω resistor limits the fault current and produces a pole at approximately 800 MHz with the effective diode capacitance of 3 pF and the AD8122 input capacitance of 1 pF. The pole drops the response by only 0.07 dB at 100 MHz and therefore has a negligible effect on the signal.

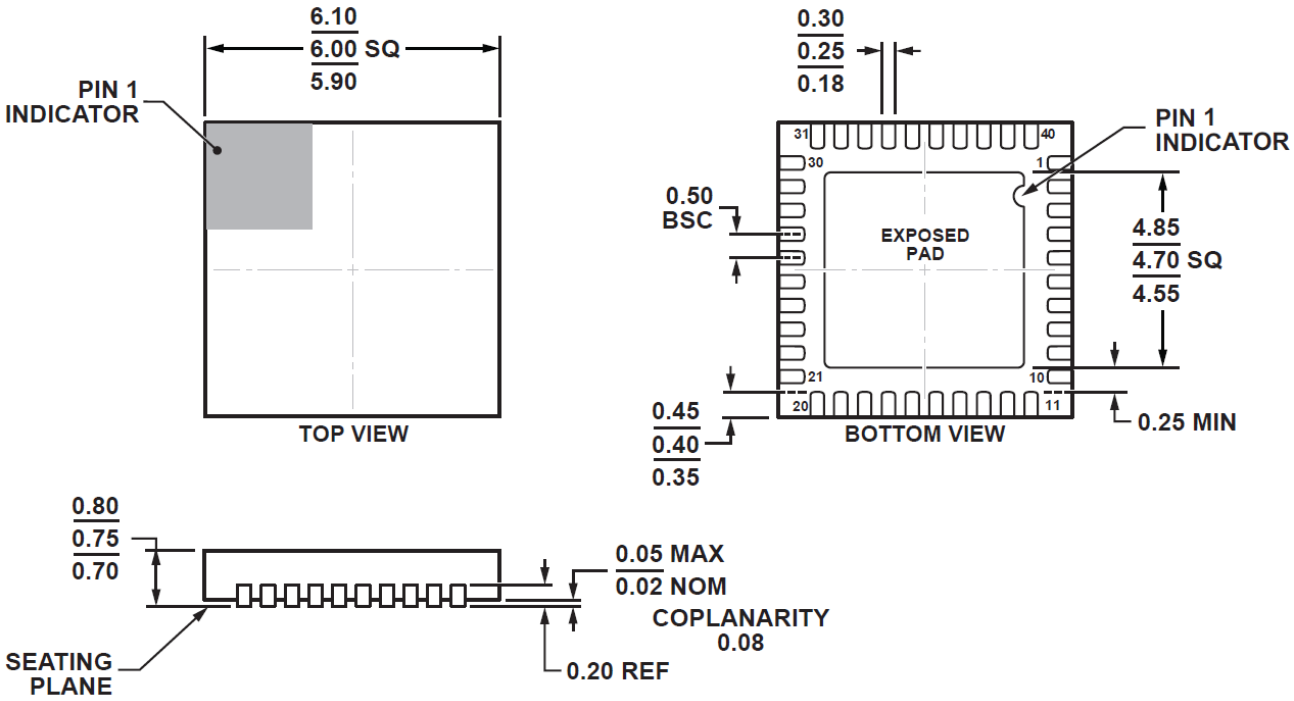
When using a single 5 V supply on the driver side, the common-mode voltage at the driver output is typically 2.5V, or fixed at 1.5V in the case of the AD8142. The largest received differential video signal is approximately 700 mV p-p, and this therefore adds 175 mV_{PEAK} to each single-ended side of the differential signal, resulting in a worst-case peak voltage of 2.675 V or 1.675 V on an AD8122 single-ended input (presuming there is no ground shift between driver and receiver). These levels are within the AD8122 input voltage swing limits, and such a system works well as long as the difference in ground potential between driver and receiver does not cause the input voltage swing to exceed these limits.

When used, common-mode sync signals are generally applied with a peak deviation of 500 mV during the blanking intervals (video = 0V), and thereby increase the common-mode level from 2.5 V to 3.0 V, or 1.5V to 2.0V in the case of the AD8142. These common-mode levels are below the upper input voltage swing limit of 4 V, and therefore leave 1 V or 2 V margin for ground shifts between driver and receiver. There are two ways to increase the common-mode range of the overall system. One is to power the driver from dual supplies (output common-mode voltage = 0 V) and the other is to place an AD8143 in front of the AD8122, as shown in Figure 9. These techniques may be combined or applied separately.

POWER-DOWN

The power-down feature is intended to be used to reduce power consumption when a particular device is not in use and does not place the output in a high-Z state when asserted. The input logic levels and supply current in power-down mode are presented in the Power Supply section of Table 1.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WJJD-5.

Figure 10. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-12)
Dimensions shown in millimeters

Pubcode: PR10780-0-5/12(PrC)